WE CLAIM:

1. An interface circuit for communicating received data from a receive clock domain into a transmit clock domain, comprising:

a buffer, comprising a plurality of entries, having an input coupled to receive data from the receive clock domain and having an output for presenting data into the transmit clock domain; and

a plurality of valid logic circuits, each associated with a corresponding one of the plurality of entries of the buffer, each valid logic circuit comprising:

a write valid latch for controlling the state of a valid line in the receive clock domain, the write valid latch having a set input coupled to receive a write request signal;

a read valid latch for controlling the state of a valid line in the transmit clock domain, the read valid latch having a reset input coupled to receive a read request signal;

reset logic for resetting the write valid latch responsive to the read request signal; and

set logic for setting the read valid latch responsive to the write request signal.

2. The interface circuit of claim 1, further comprising:

write pointer logic for maintaining a write pointer indicating one of the entries of the buffer into which a next received data word is to be written from the receive clock domain; and

read pointer logic for maintaining a read pointer indicating one of the entries of the buffer from which a next data word is to be read into the transmit clock domain.

3. The interface circuit of claim 1, wherein the reset logic comprises:

a first edge detector circuit, for detecting a transition of the read request signal in the transmit clock domain; and

a first synchronizer circuit, having an input coupled to the first edge detector circuit, for generating, at an output coupled to a reset input of the write valid latch, a reset signal synchronized into the receive clock domain.

4. The interface circuit of claim 3, wherein the set logic comprises:

a second edge detector circuit, for detecting a transition of the write request signal in the receive clock domain; and

a second synchronizer circuit, having an input coupled to the second edge detector circuit, for generating, at an output coupled to a set input of the read valid latch, a set signal synchronized into the transmit clock domain.

5. A method of transferring data words from a receive clock domain into a transmit clock domain, comprising the steps of:

applying a data word to an input of a buffer having a plurality of entries;

responsive to a write valid bit associated with a first one of the plurality of entries indicating that the first one of the plurality of entries does not contain valid data, the first one of the plurality of entries indicated by a current value of a write pointer:

storing the applied data word into the first one of the plurality of entries;

setting the write valid bit associated with the first one of the plurality of entries; and

setting a read valid bit associated with the first one of the plurality of entries; and

responsive to a read valid bit associated with a second one of the plurality of entries indicating that a second one of the plurality of entries contains valid data, the second one of the plurality of entries indicated by a current value of a read pointer:

reading the contents of the second one of the plurality of entries into the transmit clock domain;

clearing the read valid bit associated with the second one of the plurality of entries; and

clearing a write valid bit associated with the second one of the plurality of entries.

6. The method of claim 5, further comprising:

after the storing step, incrementing the write pointer.

7. The method of claim 6, further comprising:

after the reading step, incrementing the read pointer.

8. The method of claim 7, further comprising:

responsive to a read valid bit associated with a second one of the plurality of entries indicating that the second one of the plurality of entries contains valid data, testing a read valid bit associated with a next one of the plurality of entries;

wherein the reading step is performed responsive to both the read valid bit associated with a second one of the plurality of entries indicating that the second one of the plurality of entries contains valid data and to the testing step determining that the next one of the plurality of entries indicates also contains valid data.

9. The method of claim 7, further comprising:

responsive to the read valid bit associated with a second one of the plurality of entries indicating that the second one of the plurality of entries does not contain valid data, issuing an idle symbol.

10. A switch system for a communications network, comprising:

a plurality of switches, each having an interface for connecting to one or more network elements;

a plurality of switch fabric devices, each comprising:

a plurality of switch interfaces, each coupled to an associated one of the plurality of switches;

a first receive ring interface, operating in a receive clock domain;

a first transmit ring interface, operating in a transmit clock domain;

a transmit clock generator circuit, for generating a clock signal for controlling the operation of the first transmit ring interface; and

a first ring path, having an input coupled to the first ring receive interface and having an output, comprising:

a buffer, comprising a plurality of entries, having an input coupled to receive data from the first receive ring interface and having an output for presenting data to the first transmit ring interface; and

a plurality of valid logic circuits, each associated with a corresponding one of the plurality of entries of the buffer, each valid logic circuit comprising:

a write valid latch for controlling the state of a valid line in the receive clock domain, the write valid latch having a set input coupled to receive a write request signal;

a read valid latch for controlling the state of a valid line in the transmit clock domain, the read valid latch having a reset input coupled to receive a read request signal;

reset logic for resetting the write valid latch responsive to the read request signal; and

set logic for setting the read valid latch responsive to the write request signal;

a second receive ring interface;

a second ring path, having an input coupled to the second ring receive interface and having an output;

a second transmit ring interface;

wherein the first receive ring interface and second transmit ring interface correspond to a first ring interface that is coupled to a ring interface of another one of

the plurality of switch fabric devices, and wherein the first transmit ring interface and second receive ring interface correspond to a second ring interface that is coupled to a ring interface of another one of the plurality of switch fabric devices, such that the plurality of switch fabric devices are interconnected into a ring.

11. The switch system of claim 10, wherein the first ring path further comprises:

a decoder, for decoding code groups received from the first receive ring interface and for presenting data words corresponding to the decoded code groups to the buffer; and

an encoder, for encoding data words read from the buffer and presenting code groups corresponding to the encoded data words to the first transmit ring interface.

12. The switch system of claim 11, wherein the first ring path further comprises:

a first multiplexer, having a plurality of inputs, and having an output coupled to the encoder;

a ring path register, having an input coupled to the output of the buffer and having an output coupled to one of the plurality of inputs of the first multiplexer;

wherein each of the plurality of switch interfaces each have an output coupled to respective inputs of the first multiplexer.

13. The system of claim 12, wherein the first ring path further comprises:

write pointer logic for maintaining a write pointer indicating one of the entries of the buffer into which a next received data word is to be written from the receive clock domain; and

read pointer logic for maintaining a read pointer indicating one of the entries of the buffer from which a next data word is to be read into the transmit clock domain.

14. The switch system of claim 13, wherein the first ring path further comprises:

a second multiplexer, having a first input for receiving an idle symbol, and having a second input coupled to the output of the buffer, and having an output coupled to the input of the ring path register, the second multiplexer for applying the idle symbol to the ring path register responsive to the valid line in the transmit clock domain for the one of the plurality of valid logic circuits indicating that the entry of the buffer corresponding to the value of the read pointer does not contain valid data.

15. The system of claim 10, wherein the reset logic comprises:

a first edge detector circuit, for detecting a transition of the read request signal in the transmit clock domain; and

a first synchronizer circuit, having an input coupled to the first edge detector circuit, for generating, at an output coupled to a reset input of the write valid latch, a reset signal synchronized into the receive clock domain;

and wherein the set logic comprises:

a second edge detector circuit, for detecting a transition of the write request signal in the receive clock domain; and

a second synchronizer circuit, having an input coupled to the second edge detector circuit, for generating, at an output coupled to a set input of the read valid latch, a set signal synchronized into the transmit clock domain.

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